

---

# Electronics for Particle Measurement(INDEX)

Hirokazu Ikeda  
ikeda@post.kek.jp

School of Mathematical and Physical Science  
The Graduate University for Advanced Studies

Aug 10, 2004

---

## Abstract

The basics of an integrated circuit are described with special emphasis placed on a charge-measurement system. The indices for the separated texts are summarized here.

## Chapter 1

### Contents

<b>1 Steps toward integrated circuit fabrication</b>	<b>1</b>
1.1 Planning . . . . .	1
1.2 Choosing a fabrication process . . . . .	2
1.3 Circuit design . . . . .	3
1.4 Mask layout design . . . . .	4
1.5 Silicon process . . . . .	6
1.6 Evaluation/Inspection . . . . .	7
1.7 Screening . . . . .	7
1.8 Packaging and assembly . . . . .	8
<b>A Notice</b>	<b>9</b>

## Chapter 2

### Contents

<b>2 Basics about a MOSFET</b>	<b>1</b>
2.1 Bibliography . . . . .	1
2.2 MOSFET . . . . .	1
2.3 Electronic properties of a MOSFET . . . . .	2
2.4 Example circuits with a MOSFET . . . . .	5
2.5 SPICE parameters for a MOSFET . . . . .	8
<b>A Getting started with SPICE</b>	<b>10</b>

# Chapter 3

## Contents

<b>3 Logic gates</b>	<b>1</b>
3.1 Inverter circuit . . . . .	2
3.2 NAND2 circuit . . . . .	3
3.3 NAND2 circuit with output inhibit . . . . .	4
3.4 AND3 circuit . . . . .	4
3.5 NOR2 circuit . . . . .	5
3.6 Tri-state output buffer . . . . .	6
3.7 Selector . . . . .	7
3.8 D-type flip-flop circuit . . . . .	8
3.8.1 Gated inverter . . . . .	8
3.8.2 Latch circuit . . . . .	8
3.8.3 Master-slave configuration . . . . .	9
3.8.4 EDFF circuit . . . . .	10
3.9 Example of a sequential circuit . . . . .	12
JTAG TAP controller . . . . .	12
<b>A Notice</b>	<b>19</b>

# Chapter 4

## Contents

<b>4 Reference circuit and current source</b>	<b>1</b>
4.1 Power rail . . . . .	1
4.2 Reference circuit . . . . .	2
4.3 Example circuits . . . . .	4
4.3.1 Power-on-reset circuit . . . . .	4
4.3.2 Analog multiplexor . . . . .	6
4.3.3 Low-voltage differential driver . . . . .	7
4.3.4 Low-voltage differential receiver . . . . .	10

# Chapter 5

## Contents

<b>5 Signal Processing for a charge-measurement system</b>	<b>1</b>
5.1 Test-pulse injection circuit . . . . .	1
5.2 Charge-sensitive preamplifier . . . . .	2
5.3 Pole-zero cancellation circuit . . . . .	3
5.4 Non-inverting amplifier . . . . .	3
5.5 Shaping amplifier circuit . . . . .	4
5.6 Entire signal chain . . . . .	4
5.7 Alternative scheme for pole zero cancellation . . . . .	8

<b>A Notice</b>	<b>10</b>
-----------------	-----------

# Chapter 6

## Contents

<b>6 Signal-to-noise ratio of the charge-measurement system</b>	<b>1</b>
6.1 Shot noise . . . . .	2
6.2 Thermal noise . . . . .	2
6.3 Flicker noise . . . . .	3
6.4 Response of the charge-measurement system to the noise . . . . .	4
6.5 Equivalent noise charge . . . . .	11
6.6 Optimization of the peaking time . . . . .	14
6.7 Capacitance matching . . . . .	14
<b>A Observing electronic noise with a SPICE simulation</b>	<b>15</b>

# Chapter 7

## Contents

<b>7 Design of the CMOS charge-sensitive preamplifier</b>	<b>1</b>
7.1 Input FET . . . . .	1
7.1.1 Strong inversion versus weak inversion . . . . .	2
7.1.2 Procedures for optimization . . . . .	3
7.2 Open-loop gain . . . . .	5
7.2.1 Charge collection efficiency . . . . .	5
7.2.2 Cascode output . . . . .	6
7.2.3 Example with practical parameters . . . . .	7
7.3 Preamplifier circuit . . . . .	9
7.4 Feed-back ratio versus open-loop gain. . . . .	10
<b>A Notice</b>	<b>14</b>

# Chapter 8

## Contents

<b>8 Resistance circuit</b>	<b>1</b>
8.1 DC restoring scheme . . . . .	1
8.2 Schematic of the resistance circuit . . . . .	2
8.3 Limitation of the resistance circuit . . . . .	5
8.4 Compensation of the leakage current . . . . .	7
8.5 Noise associated with the leakage-current compensation circuit . . . . .	11

# Chapter 9

## Contents

<b>9 Signal processing with a discrete time domain</b>	<b>1</b>
9.1 Discrete time signal processing . . . . .	1
9.2 Double-correlated sampling . . . . .	2
9.2.1 Noise reduction with an incomplete integrator . . . . .	3
9.2.2 Noise reduction with a complete integrator . . . . .	3
9.3 General approach for discrete signal processing . . . . .	4

9.4	Reconstruction of the input-signal series . . . . .	5
9.4.1	Signal reconstruction with RC filter . . . . .	5
9.4.2	Signal reconstruction with a CR-RC filter . . . . .	6
9.5	Evaluation of the input equivalent noise charge . . . . .	7
9.5.1	Contribution of the parallel noise . . . . .	7
9.5.2	Contribution of the series noise . . . . .	8
9.6	Reconstruction of the asynchronous input signal series . . . . .	11
9.7	Resolution of the reconstructed signal series . . . . .	12
9.7.1	Amplitude resolution . . . . .	12
9.7.2	Timing resolution . . . . .	13
9.7.3	Examples . . . . .	13

以上