Introduction to Analog-VLSI Design

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Contents for talk

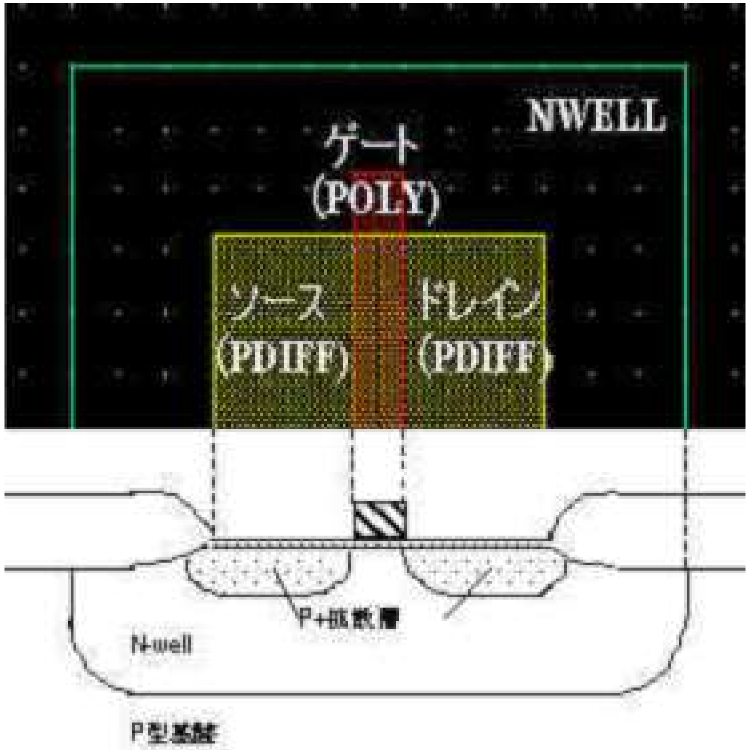
Title: Introduction to analog-VLSI design

1) What is CMOS?
2) Design flow (with examples)
3) Multi-chip project provided by VDEC
4) Recent progress: IP and Pixel

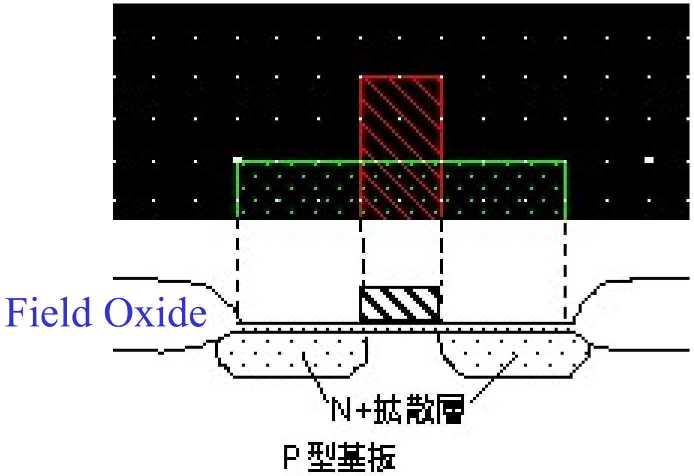
What is CMOS?(1)

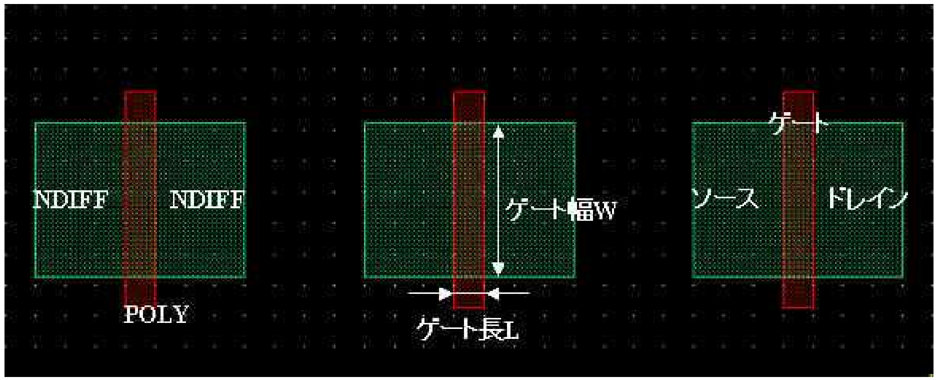
CMOS is a silicon-based integrated circuit fabrication technology with complementary FETs

PMOS Transistor



NMOS Transistor





What is CMOS?(2)

General:

1)Conformance with very high integration with very low power consumption.

2) Complicated analog-digital circuits are allowed to be mixed together

3) Fabrication process is well matured.

4) Easy to be destructed by static discharge

5) Difficult to implement large capacitors and high resistors.

6) Allowable power-rail voltage is relatively low.

7)Absolute value for elements is very poor, while matching is excellent.

8) Radiation tolerance is being improved.

Specific parameters for 0.35um CMOS from RHOM

Gate oxide : 7.2 nm

Gate length : 0.4 μm

Metal width : 0.6 μm

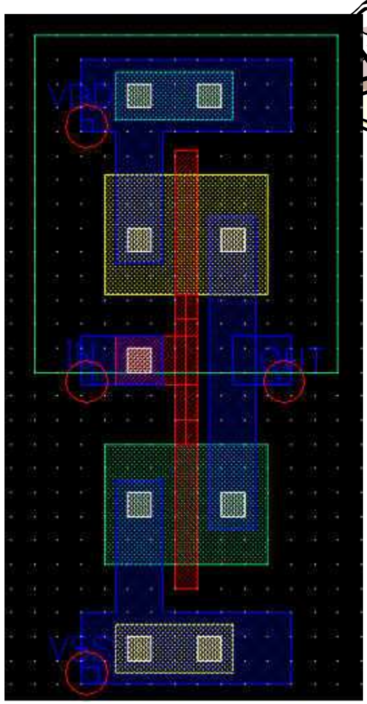
Metal spacing : 1 μm

Resistor : 2.35 kΩ/☐

Capacitor : 1.8 fF/μm^2

Power rail : 2.7-3.6 V

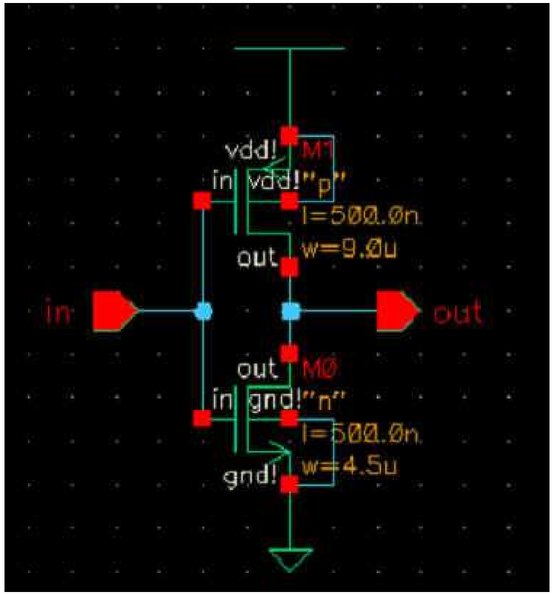
Design Flow



1)Making-up Spec's

2)Functional description

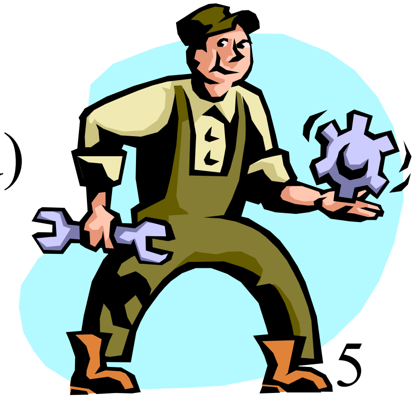
3)Transistor-based description+verification



4)Layout design +verification

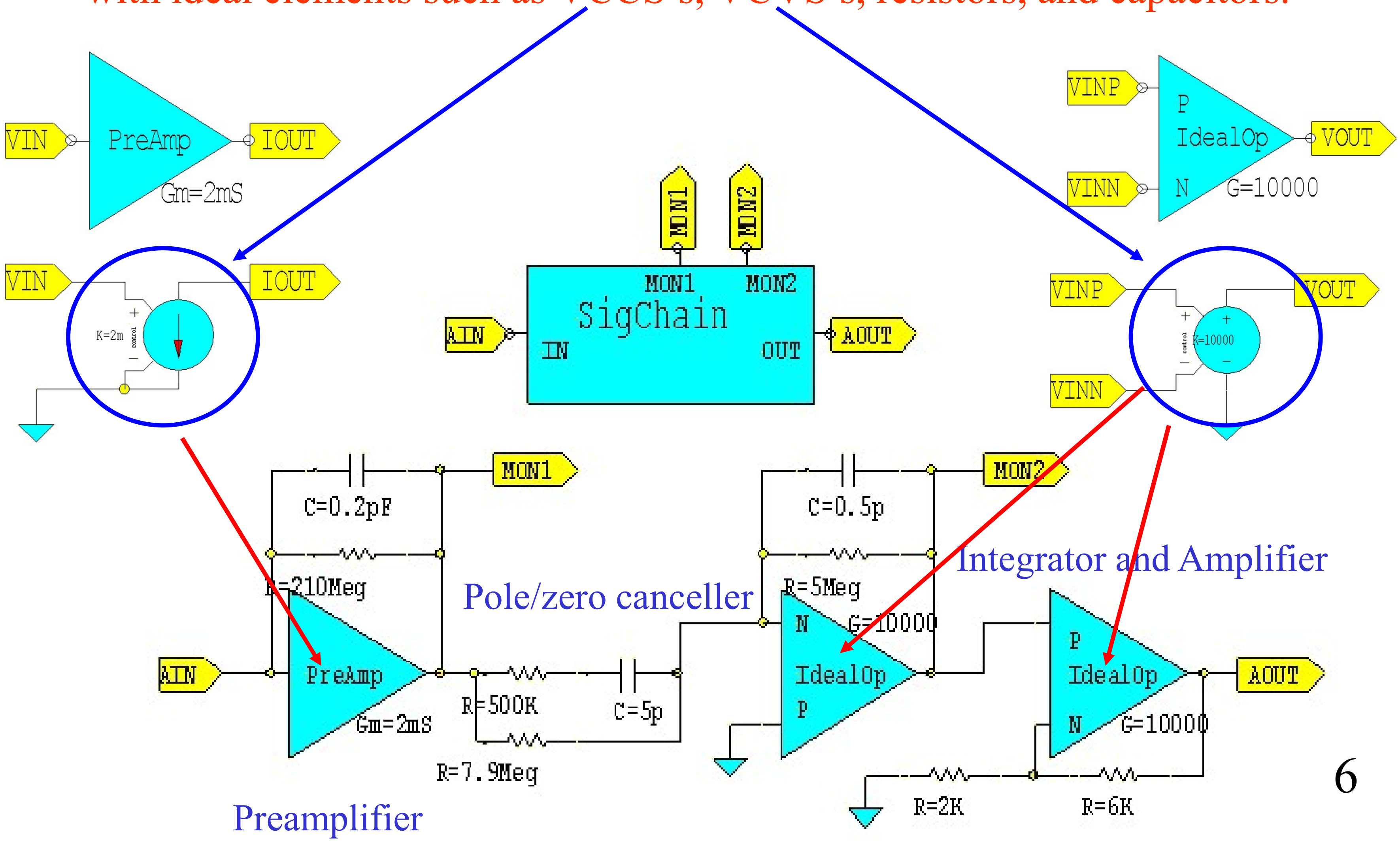
5)Silicon Process (front-end, back-end)

6)Delivery to designers



Functional Description(1)

The first step of circuit design is to construct a signal chain
with ideal elements such as VCCS's, VCVS's, resistors, and capacitors.

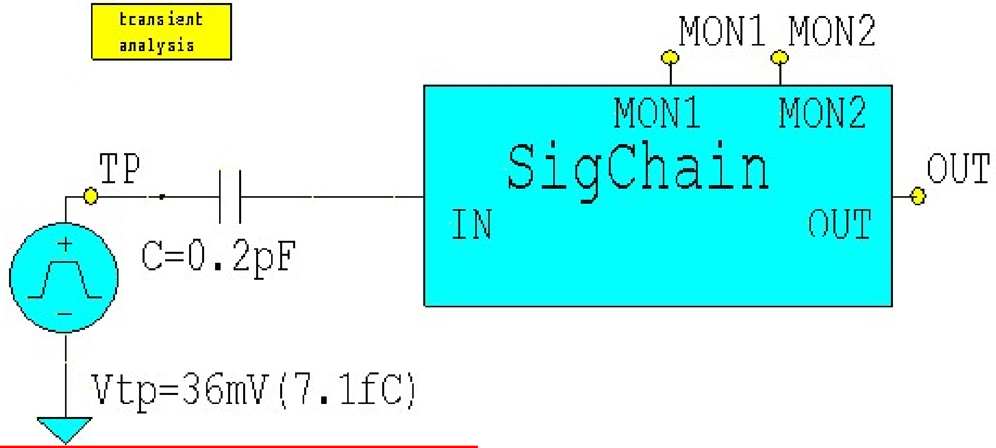


Functional Description(2)

Generation of SPICE-netlist

Simulation Program,
Integrated Circuit Emphasis

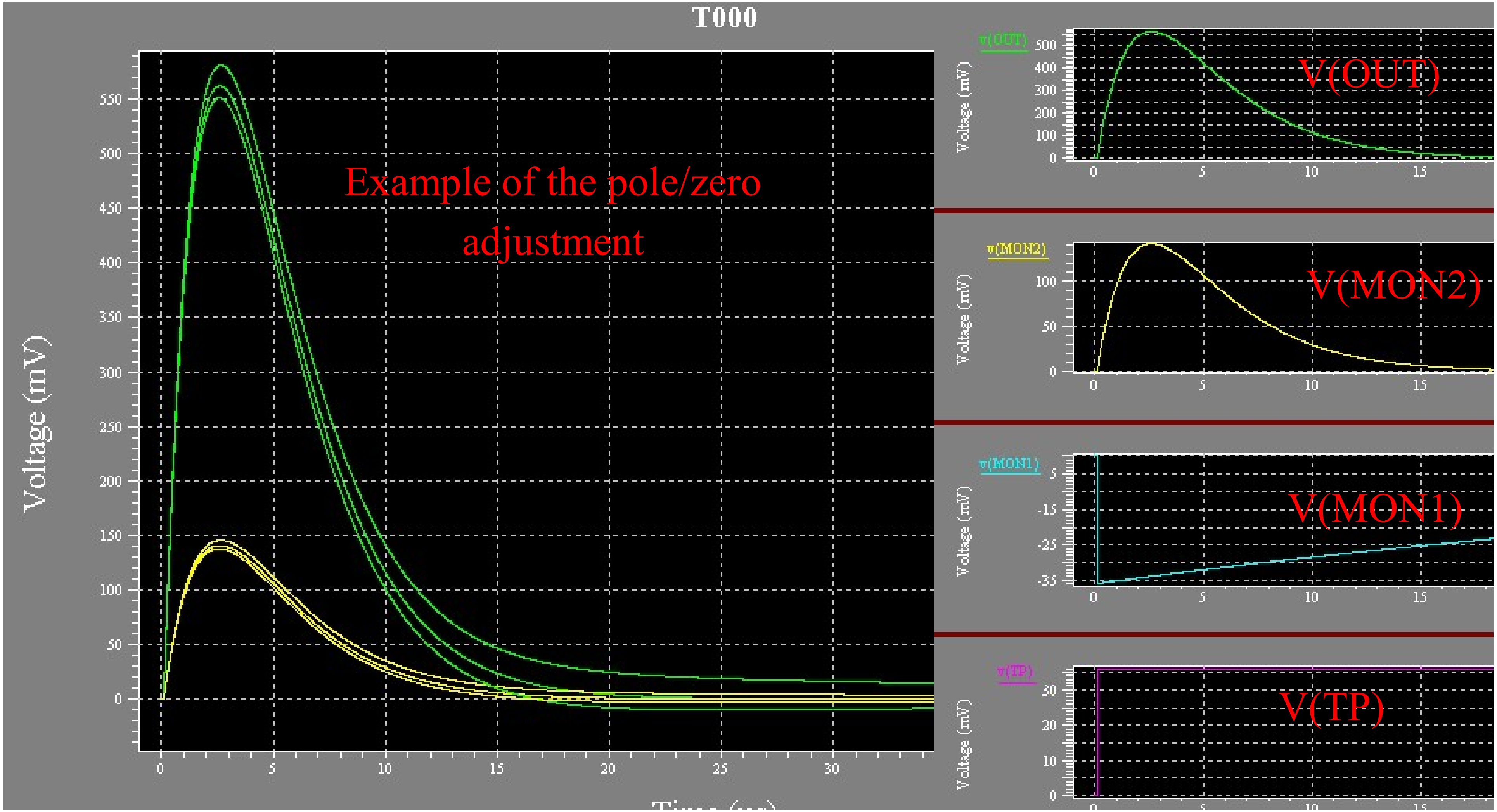
```
* SPICE netlist written by S-Edit Win32 7.03
.SUBCKT IdealOp VINN VINP VOUT Gnd
e1 VOUT Gnd VINP VINN 10000
.ENDS
.SUBCKT PreAmp IOUT VIN Gnd
g1 IOUT Gnd VIN Gnd 2m
.ENDS
.SUBCKT SigChain AIN AOUT MON1 MON2 Gnd
X1 MON1 AIN Gnd PreAmp
X2 N3 Gnd MON2 Gnd IdealOp
X3 N1 MON2 AOUT Gnd IdealOp
C1 AIN MON1 0.2pF
C2 N2 N3 5p
C3 N3 MON2 0.5p
R4 AIN MON1 210Meg TC=0.0, 0.0
R5 N3 MON2 5Meg TC=0.0, 0.0
R6 N1 AOUT 6K TC=0.0, 0.0
R7 Gnd N1 2K TC=0.0, 0.0
RP MON1 N2 500K TC=0.0, 0.0
RZ MON1 N3 7.9Meg TC=0.0, 0.0
.ENDS
```




```
* Main circuit: T000
X1 N1 OUT MON1 MON2 Gnd SigChain
C1 TP N1 0.2pF
.op
v2 TP Gnd pulse(0.0 36m 100n 10n 10n 100u 200u)
.tran 10n 50u
.print tran v(VTP) v(MON1) v(MON2) v(OUT)
* End of main circuit: T000
```

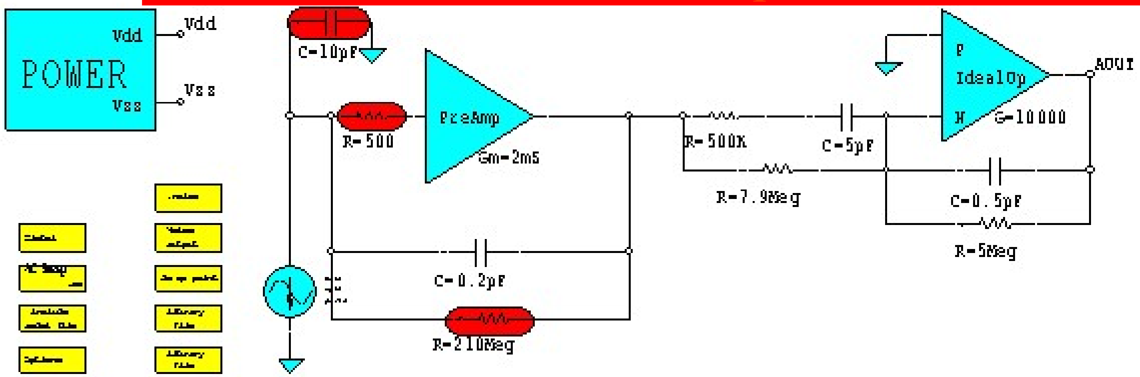
Functional Description(3)

Execution of SPICE with functional description; confirming whether the description is exactly what you want to do.

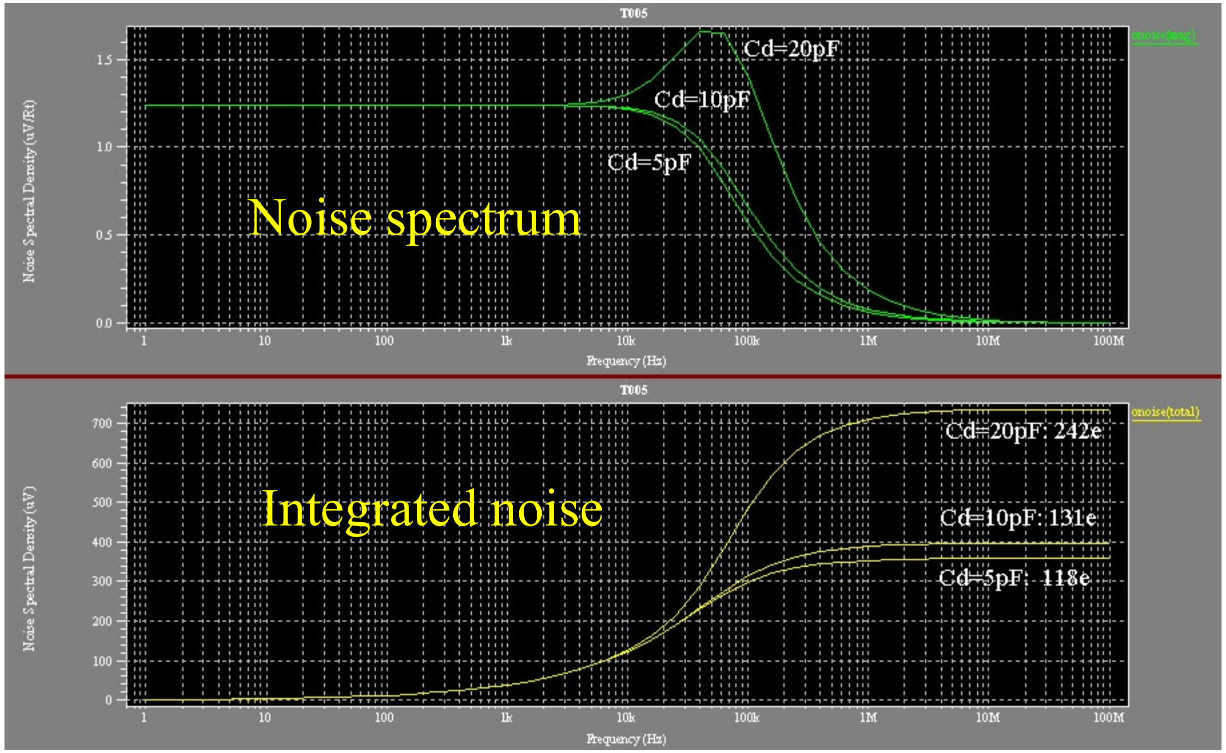


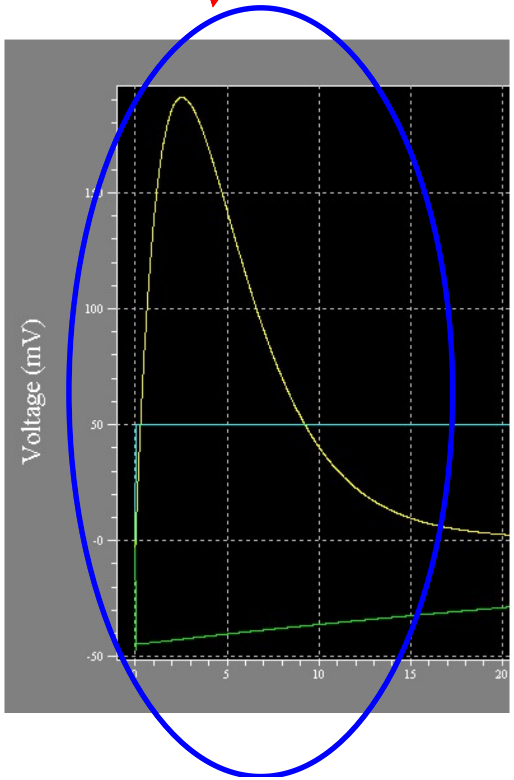
Functional description(4)

Electronic noise is inherent to electronic devices and is enhanced by detector capacitance and leakage current.



Calibration
Pulse for normalization





Transistor-based circuit design

The step is to assemble MOSFET's to implement required functions as specified or implied

1) W/O large capacitors, and high resistors
2) DC, AC, Transient, & Noise analysis
for circuit blocks, signal chains, and finally entire chip.
2) Analysis with SKEW(FAST, TYPICAL, SLOW) parameter is a mandatory part .
3) Monte-Carlo analysis is available if required.
4) Temperature dependence, power-rail dependence, and/or bias current sensitivities should be checked out as a part of final confirmation.

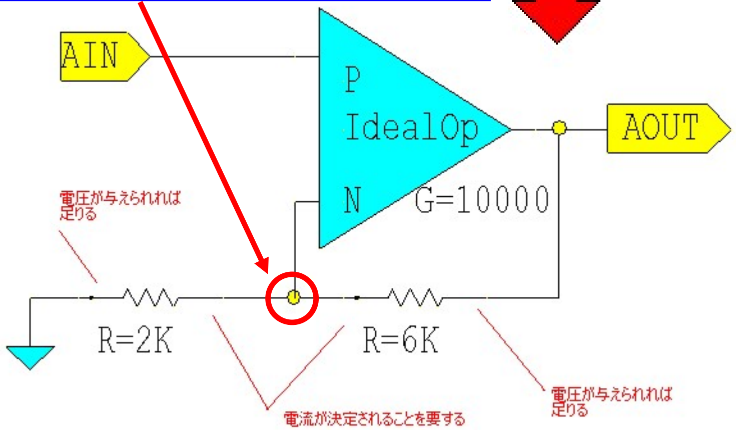
Resistance Circuit(1)

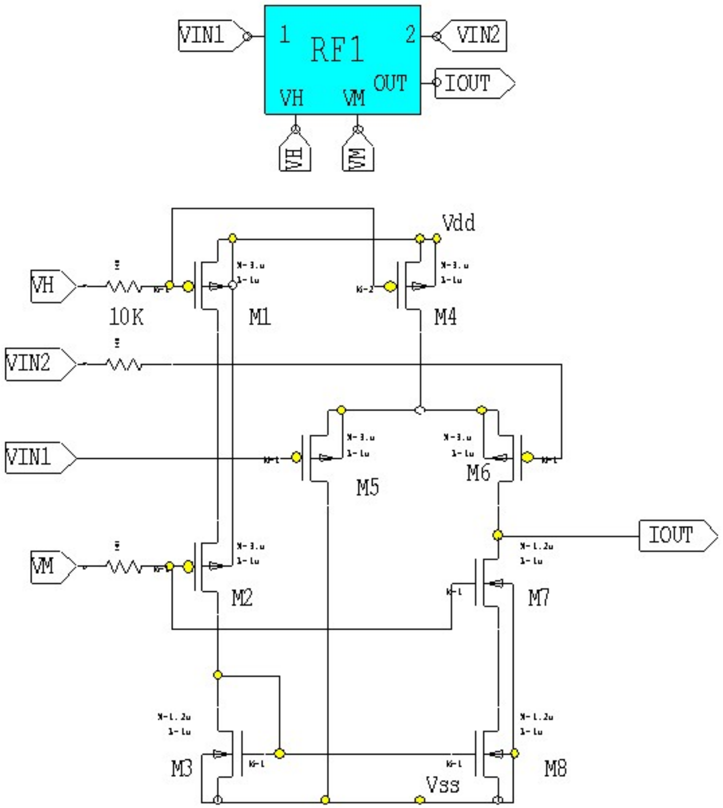
The resistance circuit exhibits a resistor-like behavior for its one terminal while the other terminal is kept as high impedance.

In general the current generated by a resistor is utilized only one terminal of the resistance device; on the other terminal the current is no more than an annoyance.

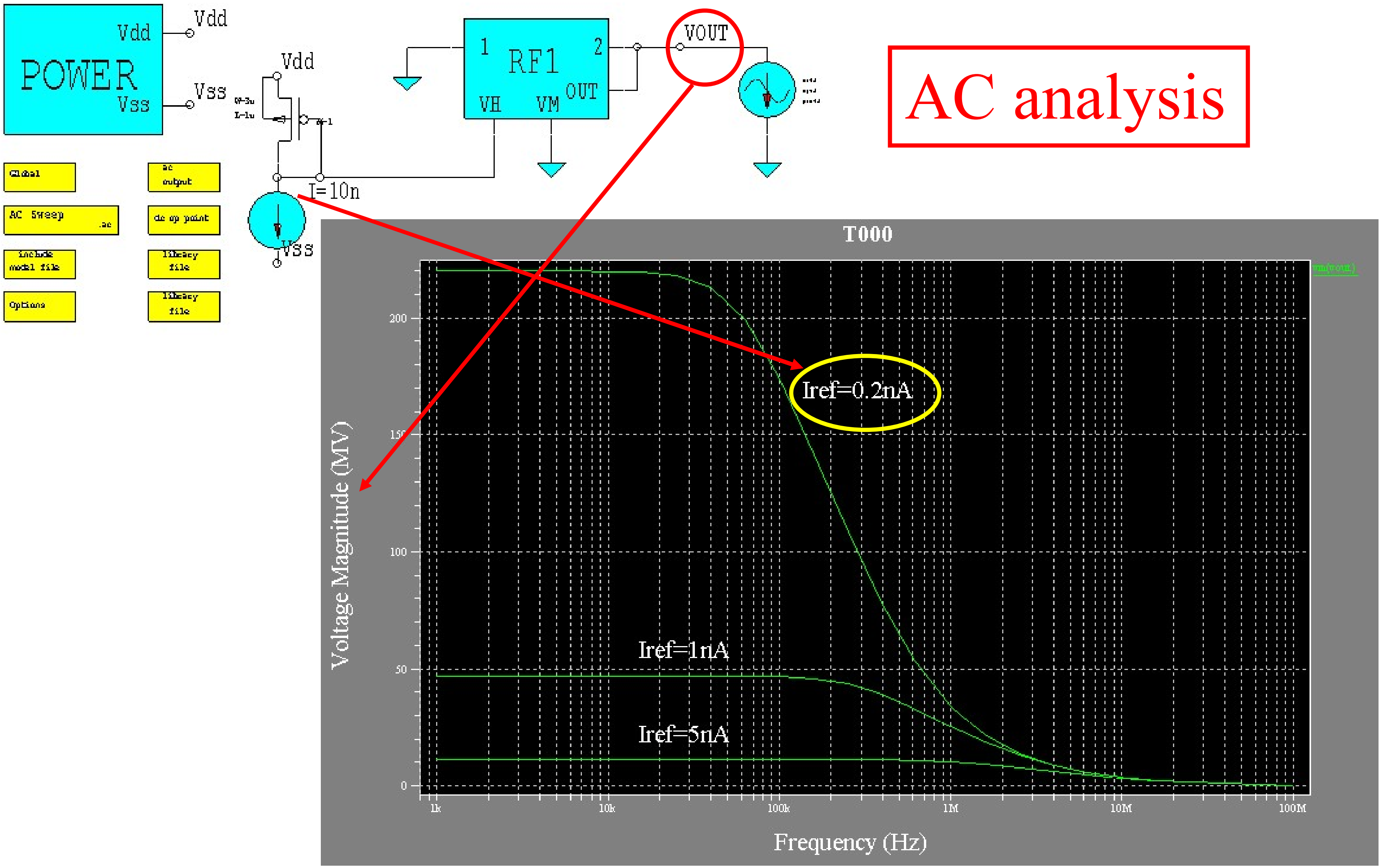
The resistance circuit can be controlled to exhibit resistance of 10kΩ to 500MΩ.

Our concern is just the KCL On this node.

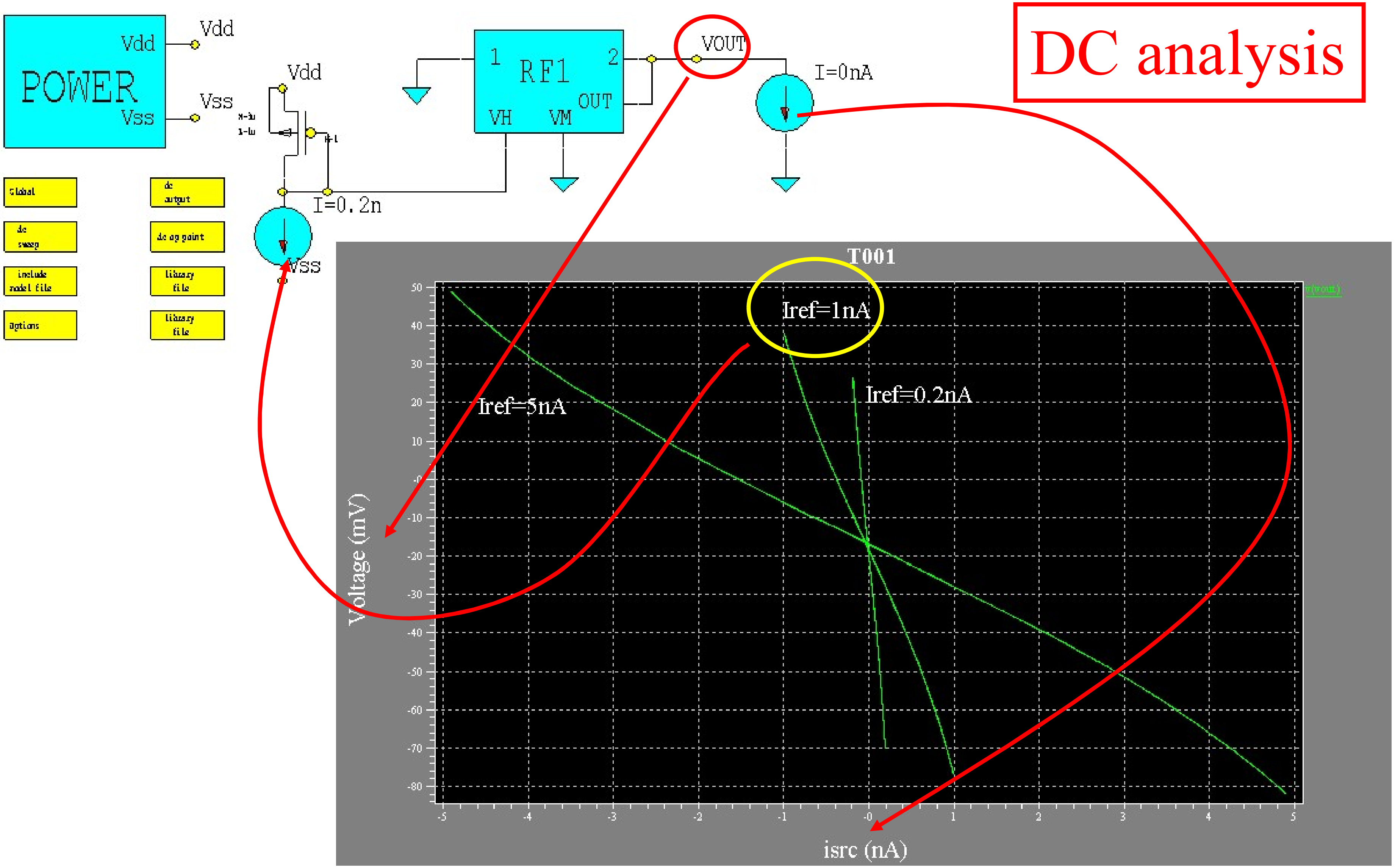




Resistance circuit(2)



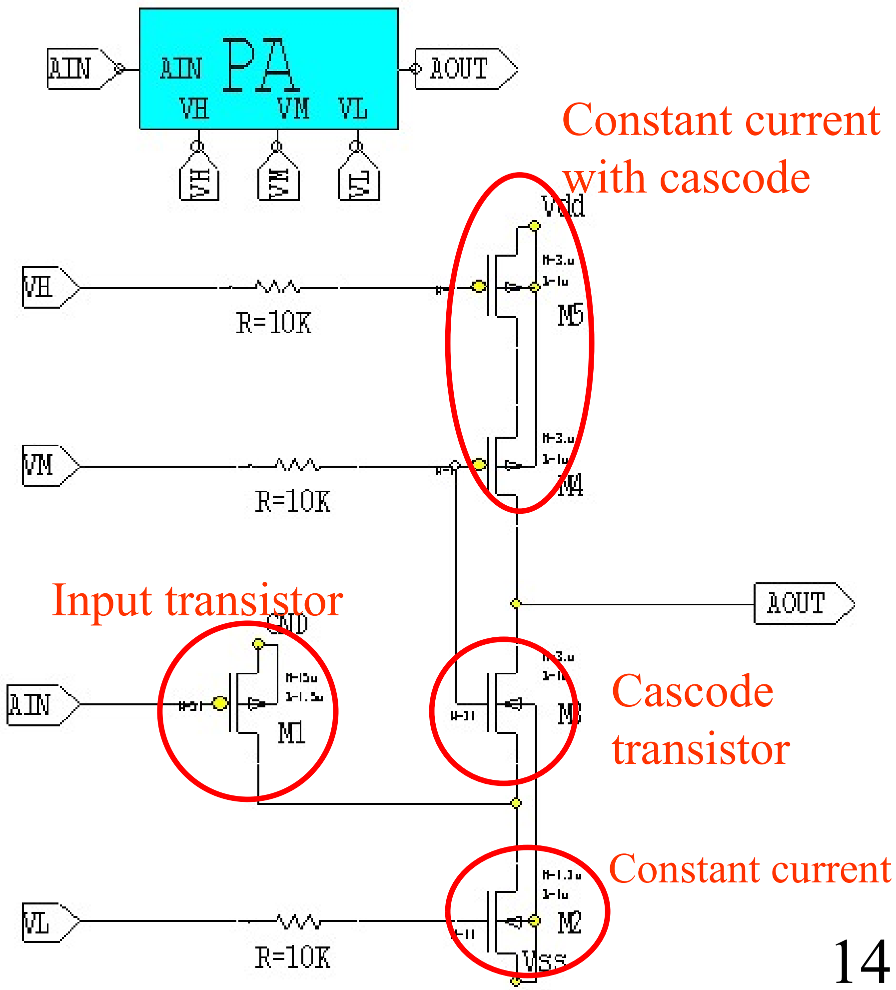
Resistance Circuit（3）



Preamplifier(1)

Preamplifier is an integrator circuit to gather charges generated in a detector medium with very low electronic noise.

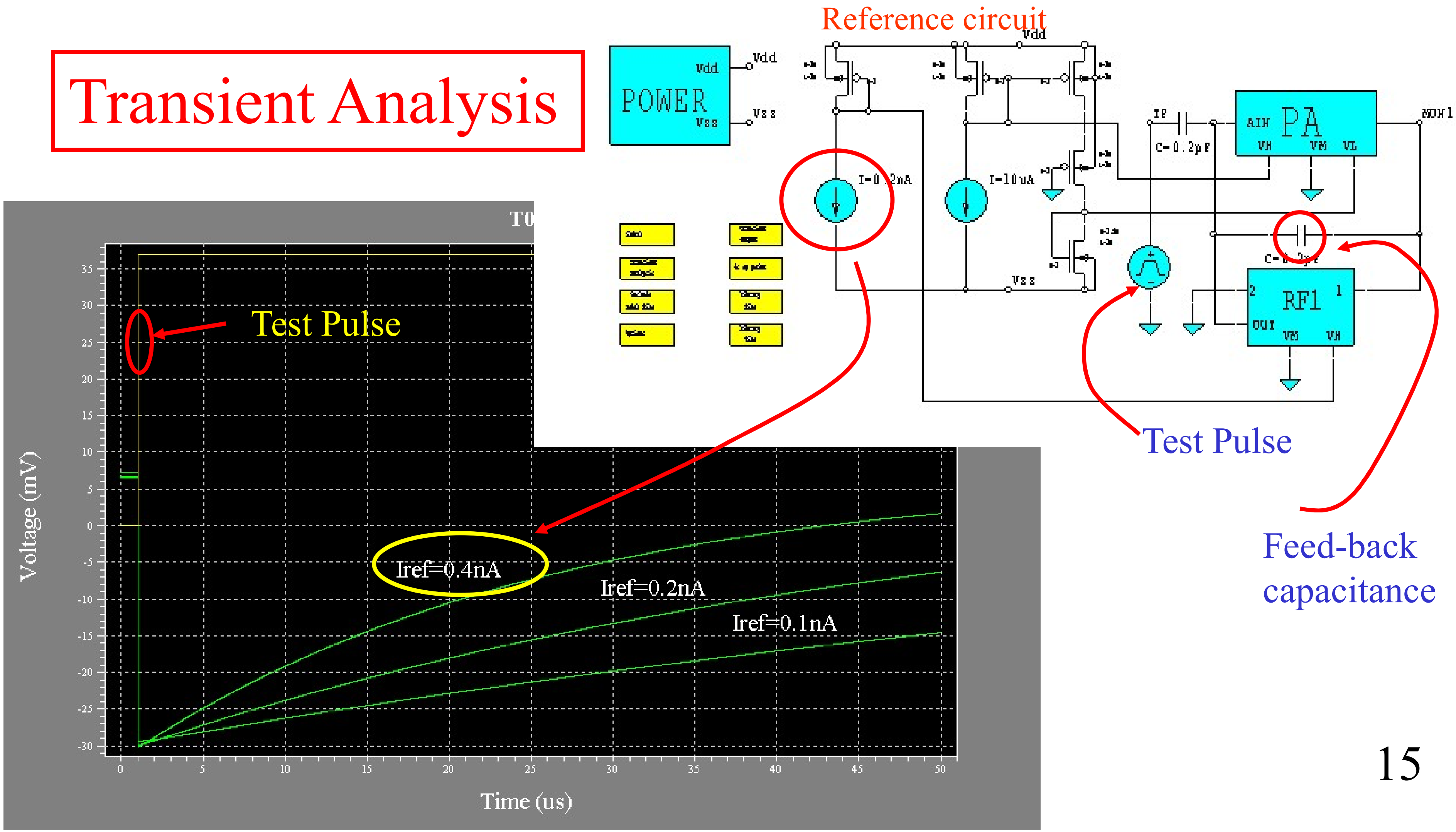
1) The input transistor employed is a pMOS with W=15um, L=0.5um, and M=50.
2)The amplifier takes a folded-cascode configuration.
3)The large input transistor suppresses electronic noise associated with the detector capacitance.
4) PMOS is known to exhibit lower 1/f noise than NMOS with less influence due to radiation.



Preamplifier(2)

Adding a resistance circuit as well as a feed-back capacitance.

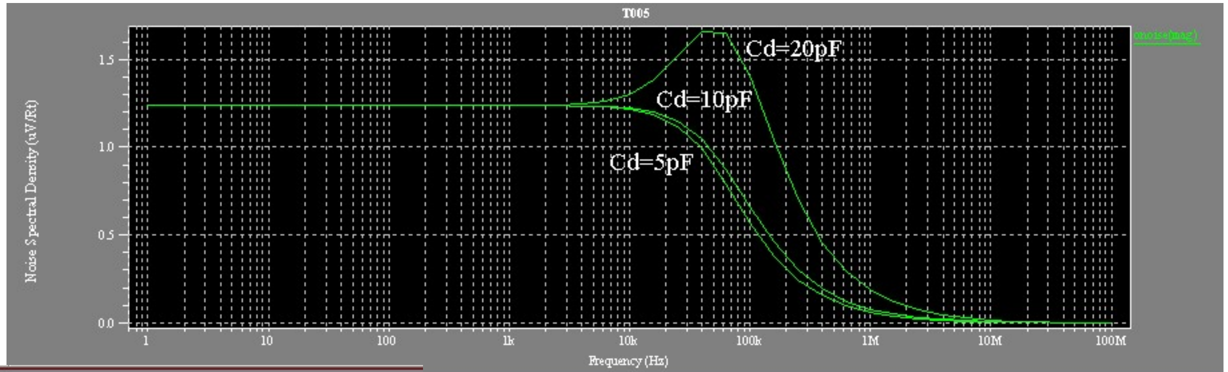
Transient Analysis

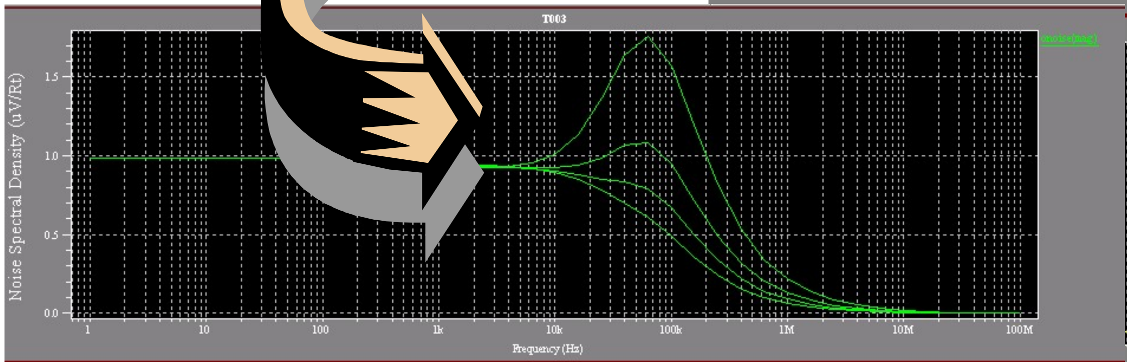


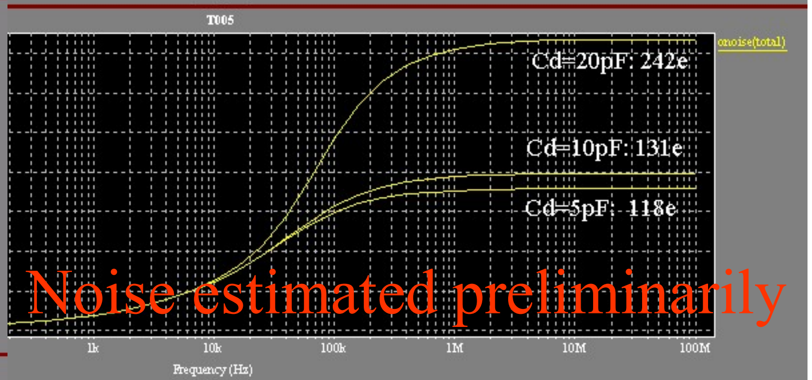
Preamplifier(3)

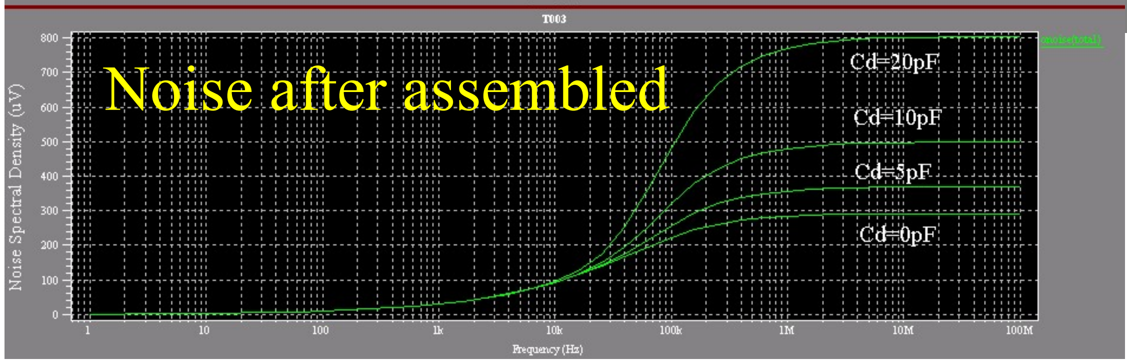
Additional noise sources contribute to the total noise in one way or another.

Noise Analysis AGAIN!







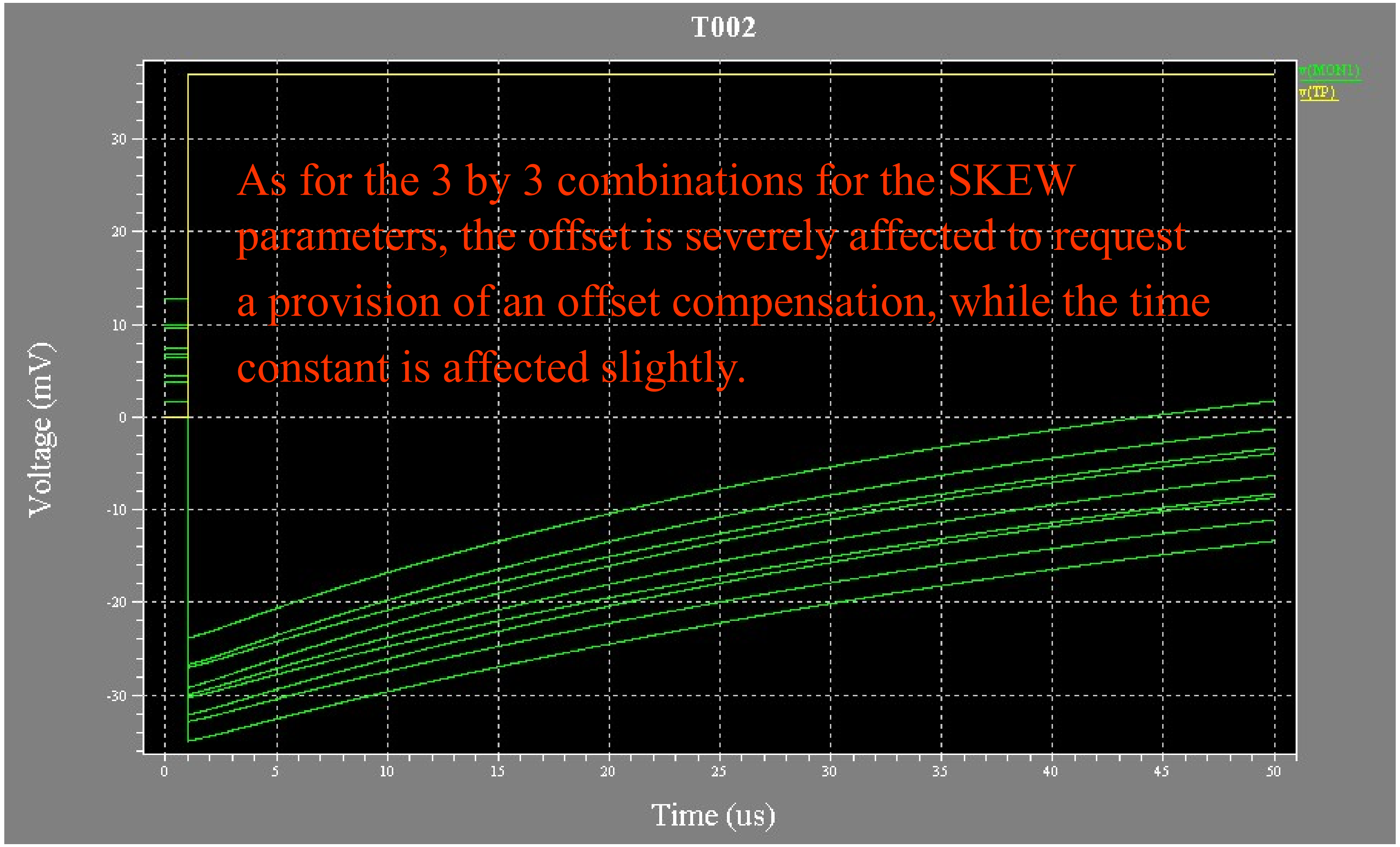


Preamplifier(4)

The SKEW parameters provide modified SPICE parameters corresponding to the deviation of the silicon process

SKEW Simulation

W/ Temperature dependence
W/ Radiation damage



As for the 3 by 3 combinations for the SKEW parameters, the offset is severely affected to request a provision of an offset compensation, while the time constant is affected slightly.

LAYOUT Design

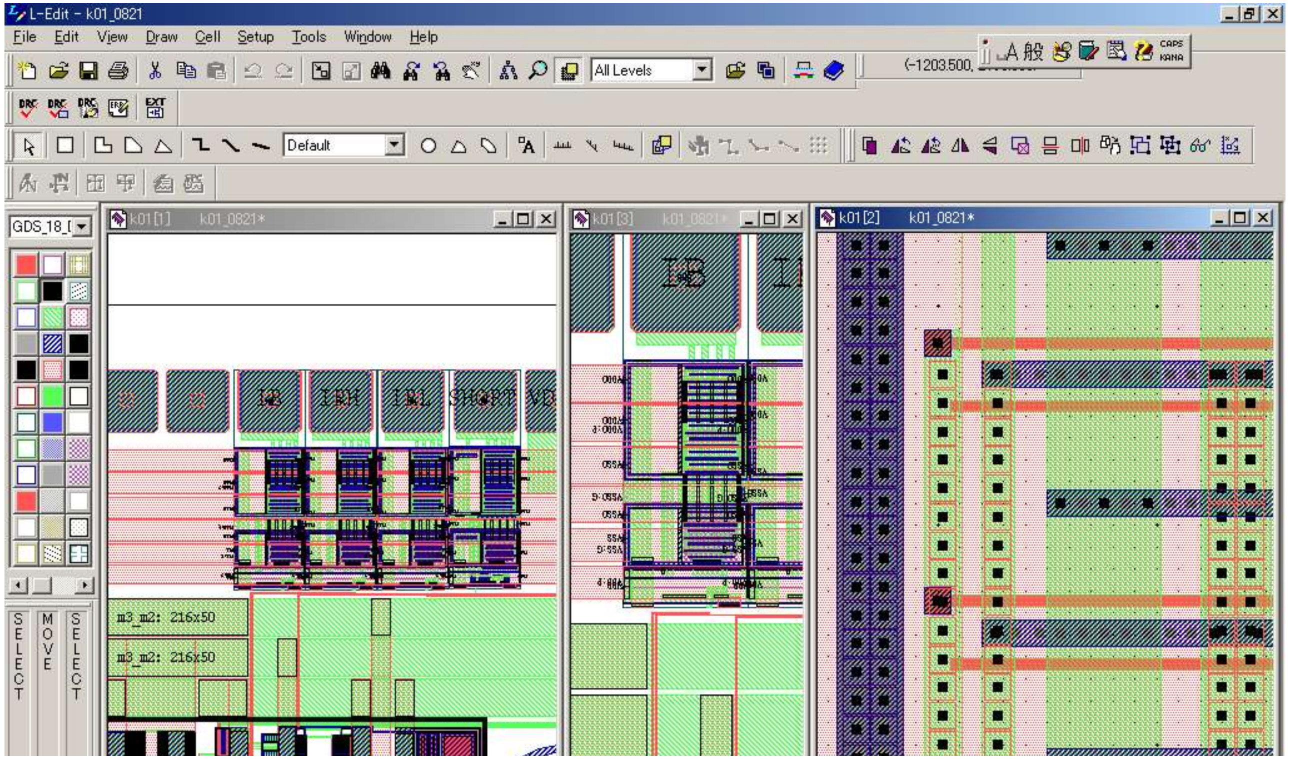
LAYOUT design is a step to draw mask geometries for a photo-lithography

It happens the case that the layout design is asked to be finished by an out-side expert; the circuit design should be well documented prior to initiating the layout design.

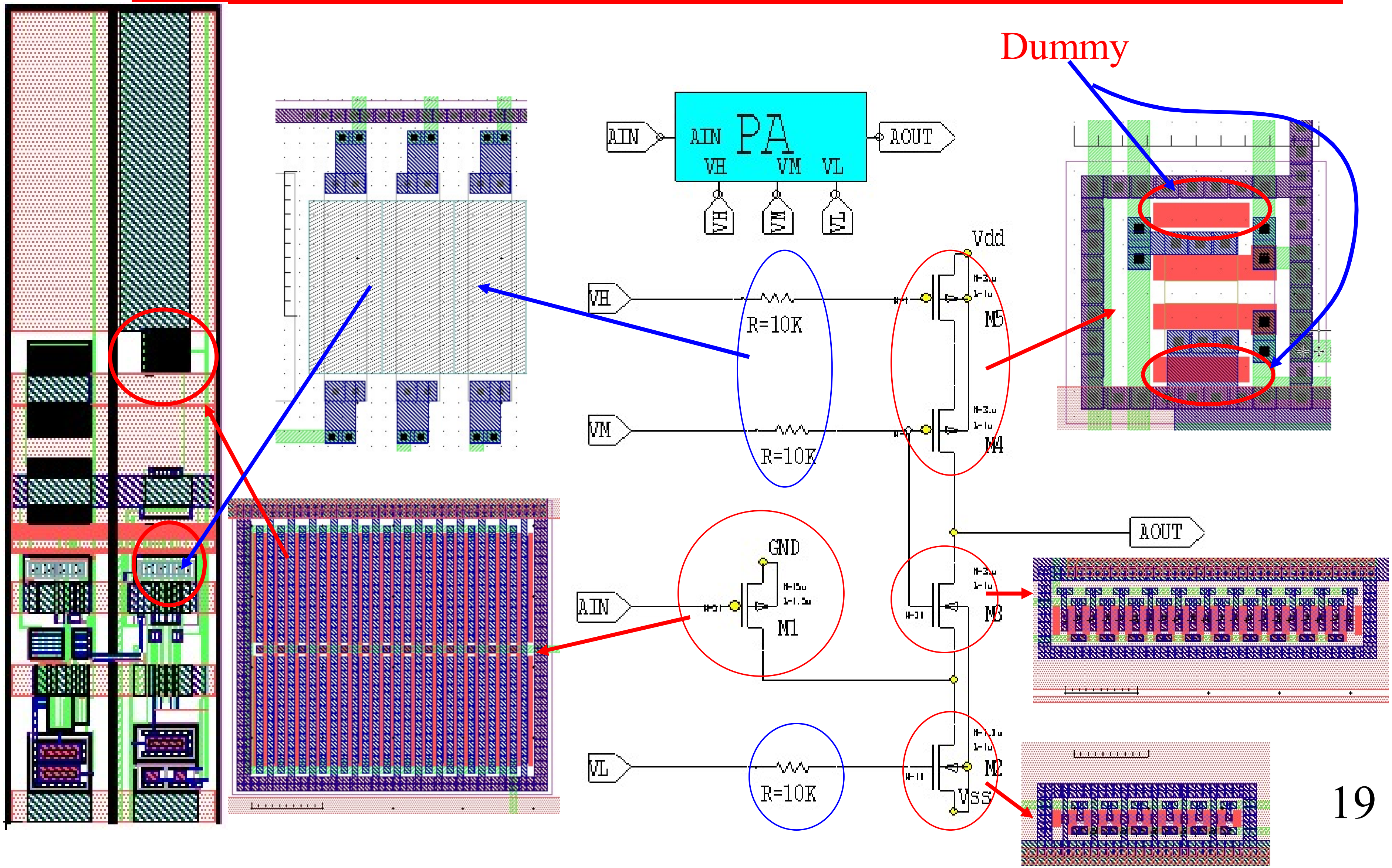
1) Examples (Preamplifier, Resistance circuit, and etc)

2) DRC

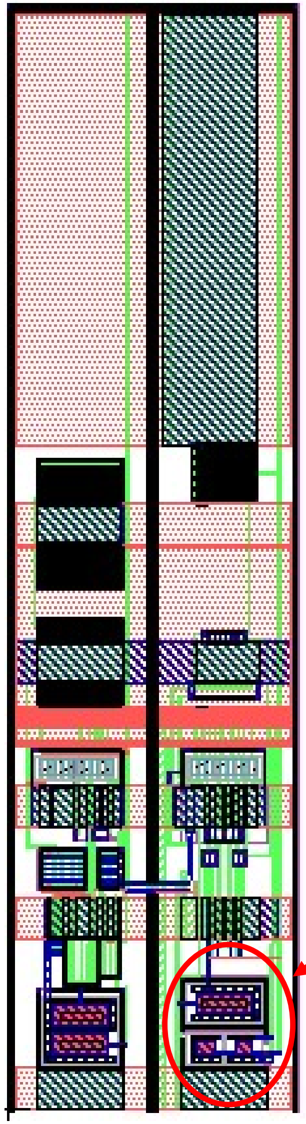
3) LVS

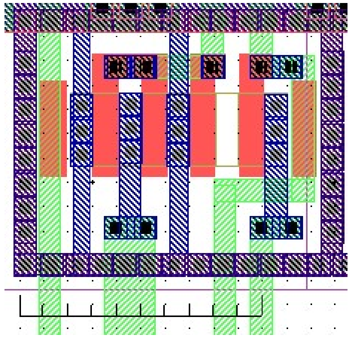


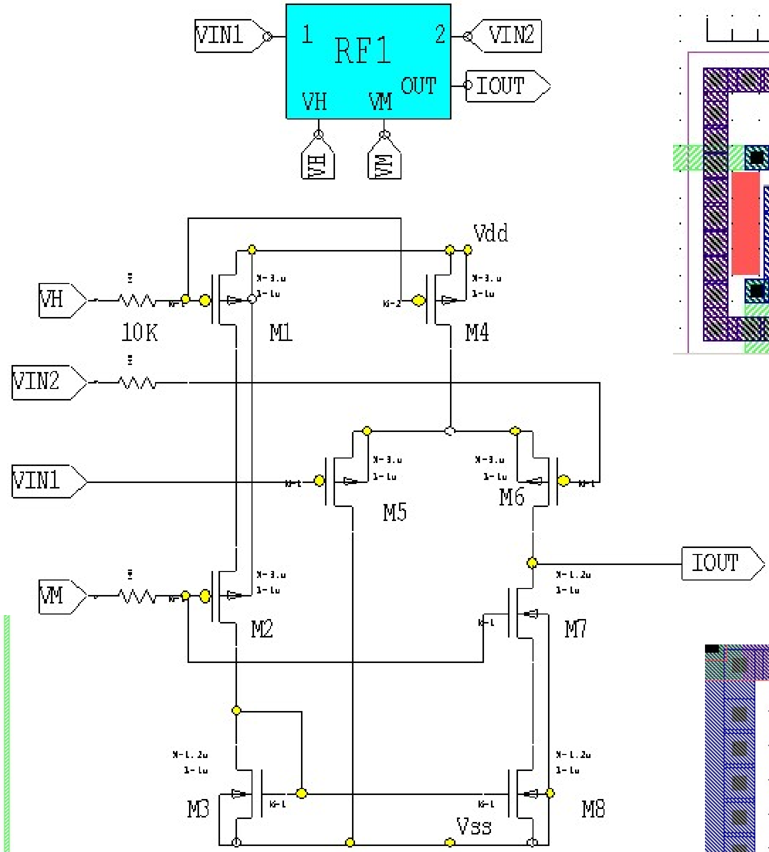
LAYOUT for Preamplifier

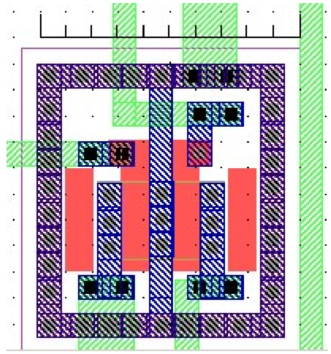


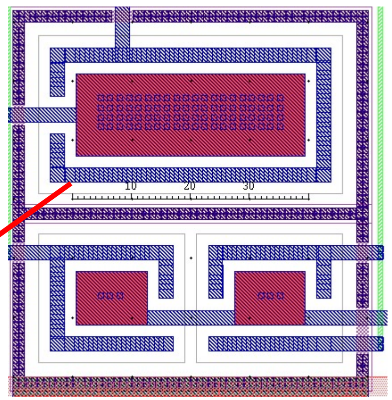
LAYOUT for Resistance Circuit

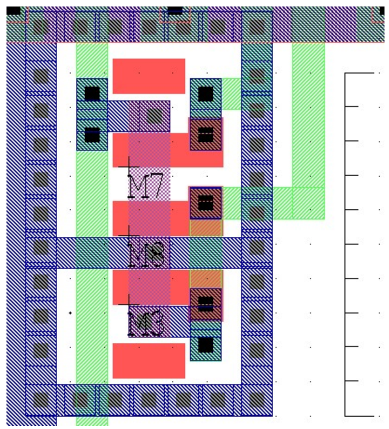






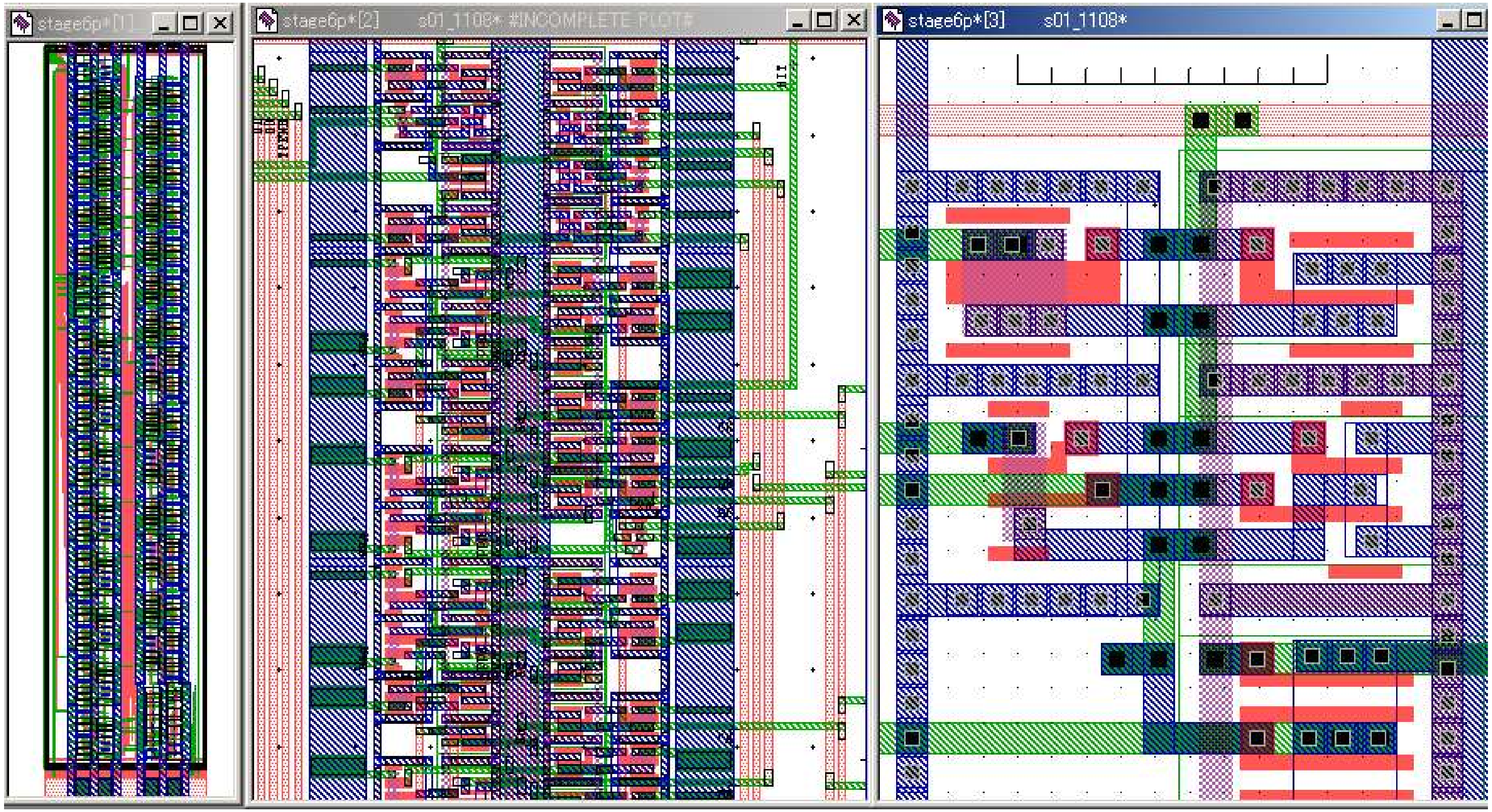






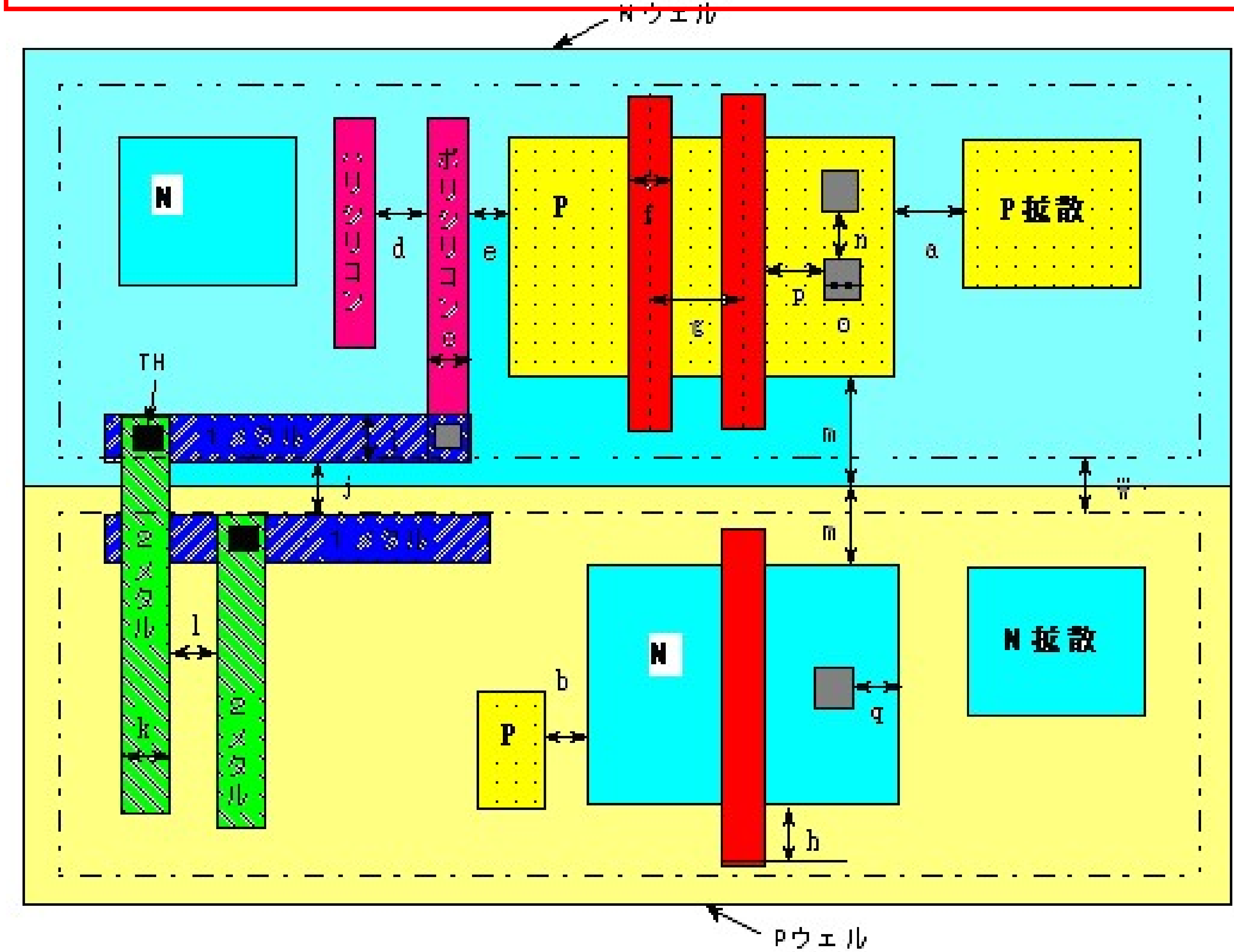
LAYOUT for Digital Circuits

Layout for digital circuits is denser than that for analog circuits



DRC

DRC is a step to eliminate violations against the design-rule.



LVS

LVS is a step to verify conformance between the layout design and the SPICE netlist.

Extracted netlist

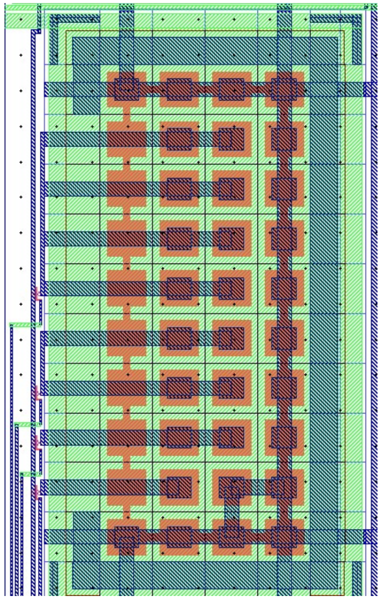
C79	VSS	16	1.99800E-13
C80	VSS	16	1.99800E-13
C81	VSS	16	1.99800E-13
C82	VSS	16	1.99800E-13
C83	VSS	17	1.99800E-13
C84	VSS	17	1.99800E-13
C85	VSS	18	1.99800E-13
C86	VSS	19	1.99800E-13
C87	VSS	16	1.99800E-13
C88	VSS	16	1.99800E-13
C89	VSS	16	1.99800E-13
C90	VSS	16	1.99800E-13
C91	VSS	17	1.99800E-13
C92	VSS	17	1.99800E-13
C93	VSS	18	1.99800E-13

STRAY CAPACITANCE

CC1	RLO	VM	2.69280E-16
CC2	RLO	VDD	3.93420E-15
CC3	RLO	AIN	7.99200E-16
CC4	RLO	VSS	1.28943E-14
CC5	VM	VDD	5.61180E-15
CC6	VM	AIN	7.99200E-16
CC7	VM	VSS	1.76425E-14
CC8	AIN	VDD	4.84440E-15
CC9	AIN	VSS	5.41248E-15
CC10	AIN	15	2.46144E-15
CC11	AIN	24	2.87500E-16
CC12	AOUT	VDD	1.59840E-15
CC13	AOUT	VSS	4.07737E-14
CC14	AOUT	C0	2.36160E-16
CC15	AOUT	C1	5.71680E-16
CC16	AOUT	C2	5.71680E-16
CC17	AOUT	C3	5.71680E-16
CC18	AOUT	13	1.20960E-15
CC19	AOUT	15	3.10768E-15
CC20	C0	VDD	6.27600E-16
CC21	C0	VSS	1.65874E-14
CC22	C0	C1	1.52280E-16
CC23	C0	C2	1.52280E-16
CC24	C0	C3	1.52280E-16
CC25	C1	VDD	6.27600E-16
CC26	C1	VSS	1.94140E-14
CC27	C1	C2	1.52280E-16
CC28	C1	C3	1.52280E-16
CC29	C2	VDD	6.27600E-16
CC30	C2	VSS	2.16160E-14
CC31	C2	C3	1.52280E-16
CC32	C3	VDD	6.27600E-16
CC33	C3	VSS	2.59496E-14
CC34	11	VDD	3.97345E-14
CC35	11	VSS	3.34900E-15
CC36	11	13	9.07200E-16
CC37	11	15	2.41920E-15
CC38	12	VDD	2.01848E-15
CC39	12	VSS	4.18735E-14
CC40	12	13	1.22085E-15
CC41	12	20	1.20960E-15
CC42	12	21	9.07200E-16
CC43	12	29	2.87500E-16
CC44	12	30	2.87500E-16
CC45	13	VDD	7.01411E-15
CC46	13	VSS	2.07688E-14
CC47	13	22	3.02400E-16
CC48	14	VDD	5.71456E-15
CC49	14	22	3.02400E-16
CC50	15	VDD	2.87840E-15
CC51	15	VSS	7.73580E-15
CC52	15	24	1.21120E-15
CC53	15	25	1.21120E-15
CC54	16	VDD	1.33974E-13
CC55	16	VSS	2.25064E-14
CC56	17	VDD	6.69872E-14
CC57	17	VSS	1.05768E-14
CC58	18	VDD	3.34936E-14
CC59	18	VSS	4.61200E-15
CC60	19	VDD	2.31392E-14
CC61	19	VSS	4.61200E-15
CC62	20	VSS	6.26770E-15
CC63	21	VSS	4.70260E-15
CC64	22	VDD	2.40430E-15
CC65	23	VDD	1.19240E-15
CC66	26	VSS	8.91600E-16
CC67	27	VSS	8.54000E-16
CC68	28	VSS	8.91600E-16
CC69	29	VSS	8.91600E-16
CC70	30	VSS	8.91600E-16

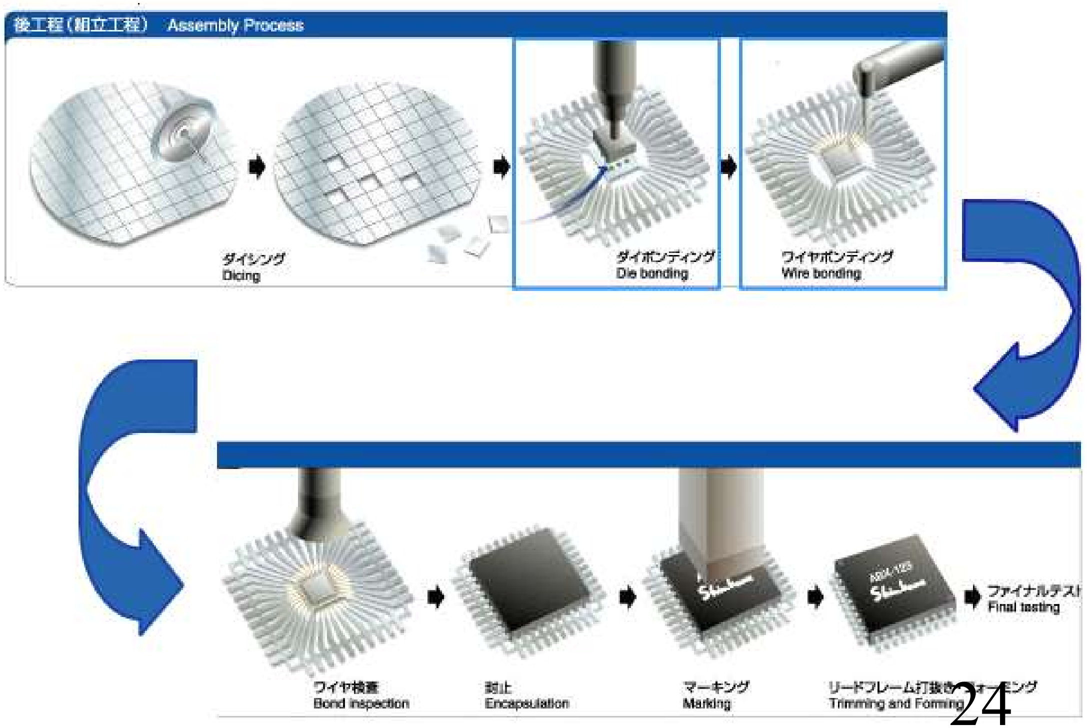
SPICE netlist

C0	N1	Vss	0.2pF
C1	N5	Vss	0.4pF
C2	N4	Vss	0.8pF
C3	N3	Vss	1.6pF



If everything is OK, the sing-off condition is met.

Silicon Process and Assembly



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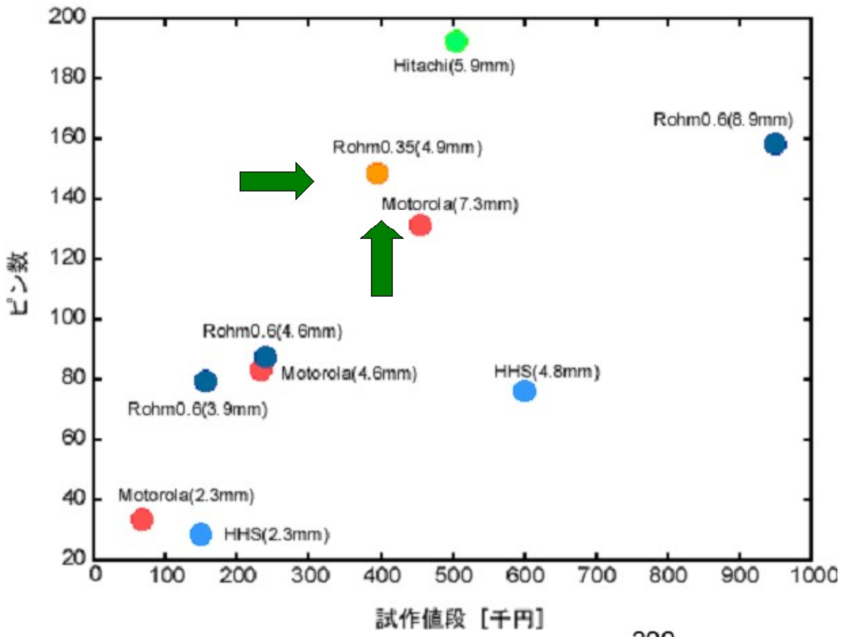
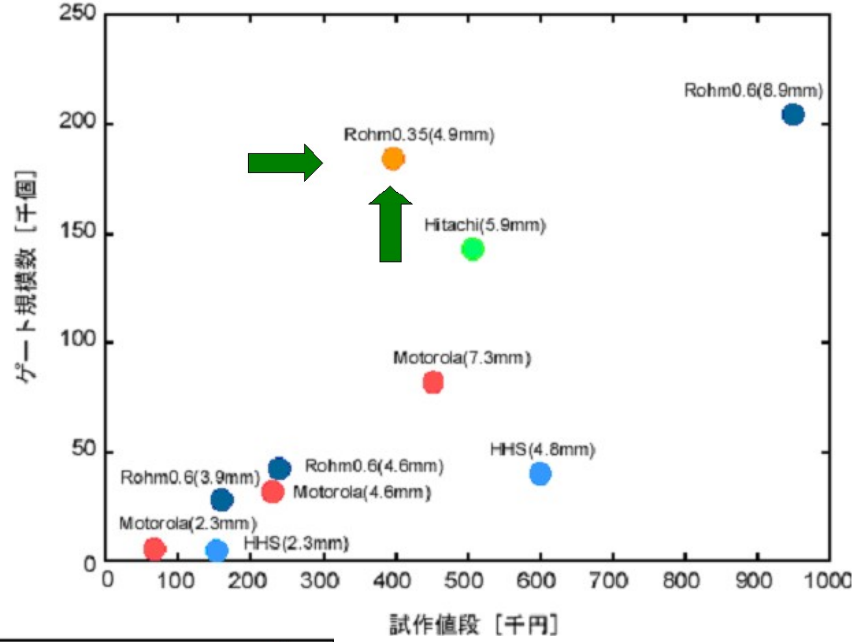
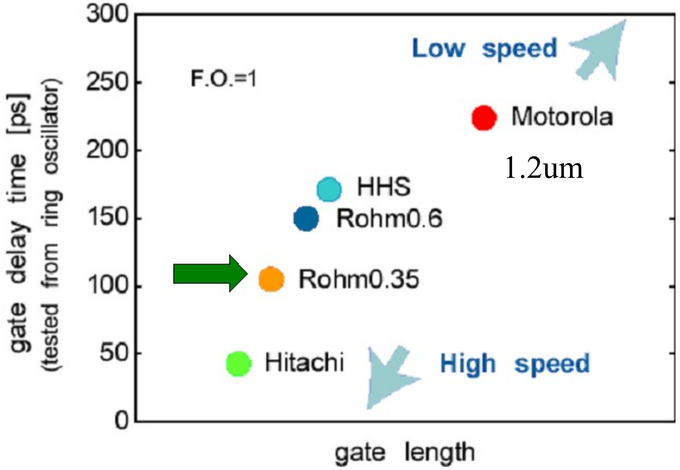






Development of front-end IP

Front-end is a circuit directly connected to a radiation detector.
IP stands for Intellectual Properties; specifically reusable sub-circuit designs organized to be ready for migrated use.

From ASIC's designed for special purpose

1) Multi-channel signal processing circuit for CdTe X-ray detector.
2) Timing/amplitude readout circuit for 3D pixel detector.
3) Digital readout circuit for HPD array device.

→

Reusable circuit blocks such as

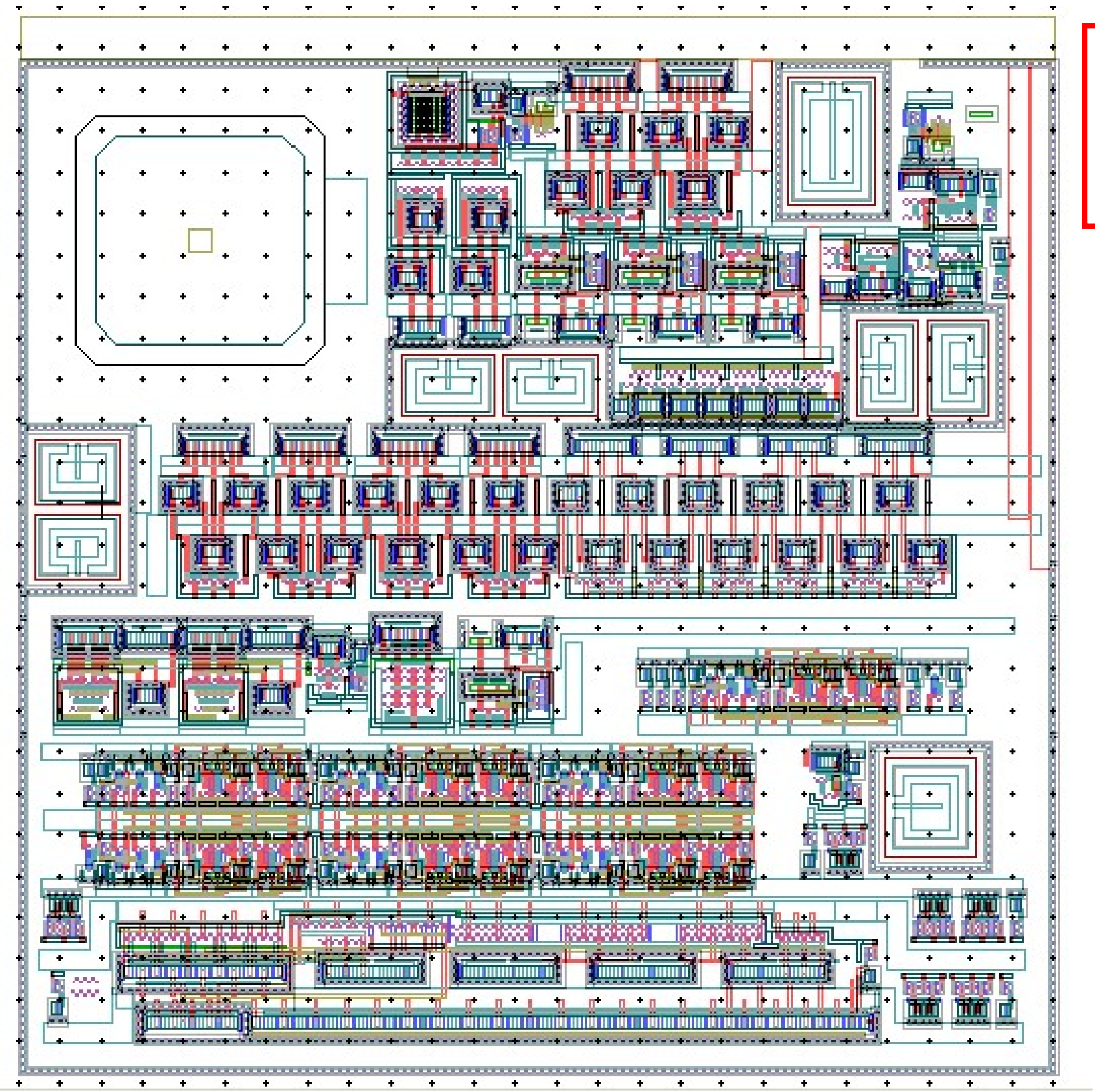
1) Amplification elements
2) Reference circuits
3) Logic gates
4) I/O pads, and etc

are extracted for later use

↓

The labor loads save in this approach are deployed for still unexplored circuit elements, which are applied for new circuit design.

Pixel readout design in progress

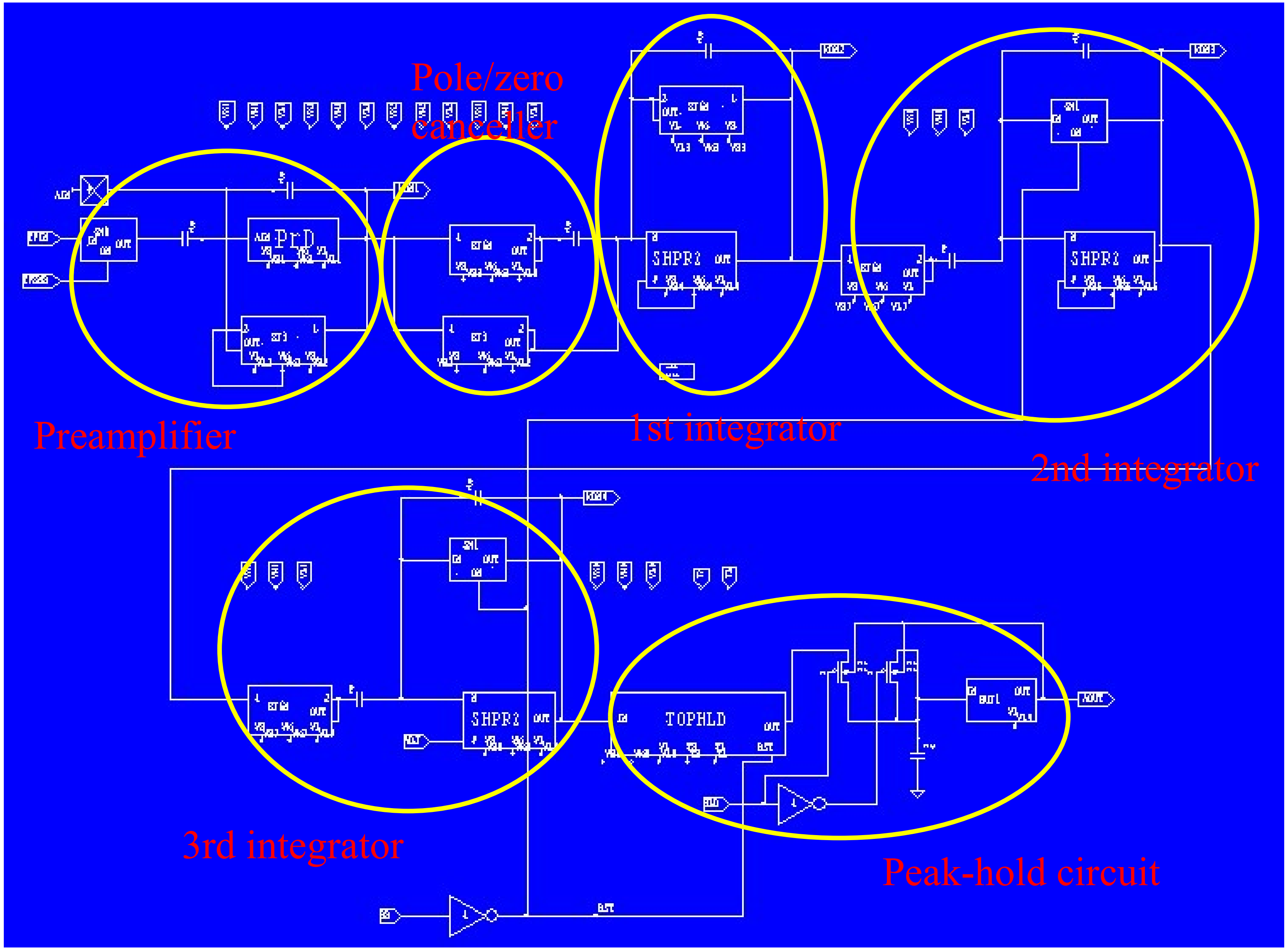


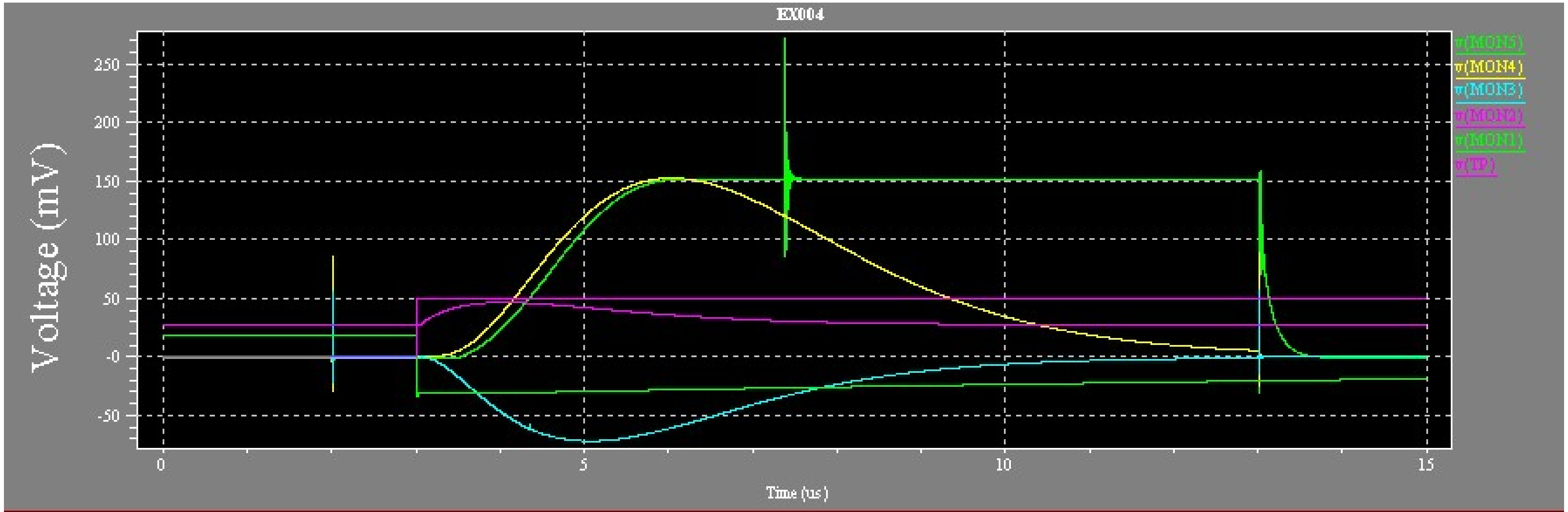
In place of Conclusion/summary

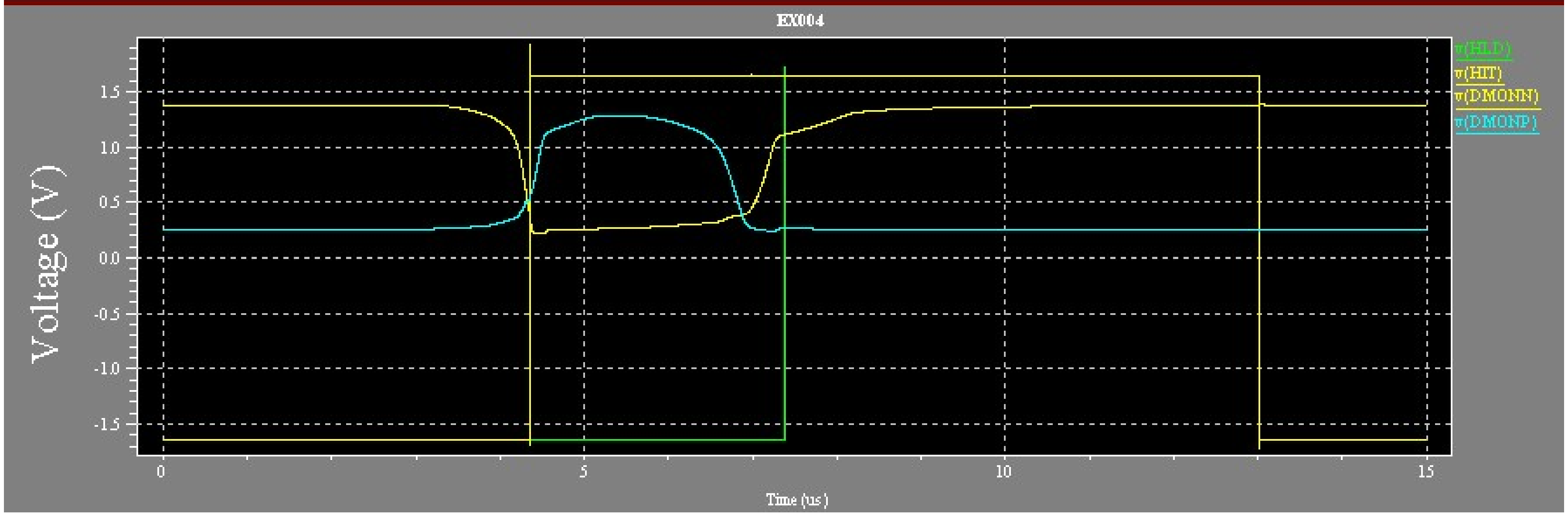
1) 260μm by 260μm
2) Preamplifier
3) Shaping amplifier CR-RC^3
4) Peak-hold circuit
5) Comparator
6) Analog multiplexer
7) Trim-DAC/registers

以上

以下付録が２枚あります。


Pole/zero
canceller
Preamplifier
1st integrator
2nd integrator
3rd integrator
Peak-hold circuit
PrD
SHPR2
SHPR2
SHPR2
TOPHLD


EX004
Voltage (mV)
Time (us)
v(MON5)
v(MON4)
v(MON3)
v(MON2)
v(MON1)
v(TP)


EX004
Voltage (V)
Time (us)
v(HLD)
v(HIT)
v(DMONN)
v(DMONP)